What is claimed is:

1. An interface for synchronous data transfer from a first domain clocked at one frequency to a second domain clocked at a slower frequency, comprising:

a first latch for receiving data from the first domain when the first latch is selected;

a second latch for receiving data from the first domain when the second latch is selected; and

a third latch for transferring data from said first latch or said second latch to the second domain when the second domain is clocked by a clock pulse, said third latch being alternately toggled to receive data from said first latch or said second latch in response to a negative edge of the clock pulse clocking the second domain.

2. The interface of claim 1, wherein a first clock clocking the first domain and a second clock clocking the second domain are both derived from a single primary clock and generate clock pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse also generated by the same primary clock.

3. The interface of claim 2, wherein at least one clock pulse of the first domain clock is a non-operate (NOP) clock pulse in each repeated systematic pattern when no data from the first domain is loaded into either said first latch or said second latch to cause equal average data transfer between the first domain and the second domain.

4. The interface of claim 3, wherein the NOP clock pulse is selected to minimize latency and prevent the slower clocked domain from being overrun by the faster clocked domain.

5. The interface of claim 1, wherein said first and second latches are alternately selected by a select signal, said select signal being generated to select one of said first or

second latches when the other of said first or second latches receives data.

6. An interface for synchronous data transfer between a first domain clocked at one frequency and a second domain clocked at a faster frequency, comprising:

a first latch for receiving data from the first domain when the first latch is selected;

a second latch for receiving data from the first domain when the second latch is selected; and

a third latch alternately toggled to receive data from said first latch or said second latch in response to a negative edge of a clock pulse, other than a hold pulse, clocking the second domain and said third latch transferring data from said first latch or said second latch to the second domain when the second domain is clocked by a next clock pulse that is not a hold clock pulse.

7. The interface of claim 6, wherein the clock pulses of the first domain and the second domain are both derived from a primary clock and repeat in a ratioed, systematic pattern framed by a secondary synch pulse.

8. The interface of claim 6, wherein the hold clock pulse is selected to minimize latency.

9. The interface of claim 6, wherein said first and second latches are alternately selected by a select signal, said select signal being generated to select one of said first or second latches when the other of said first or second latches receives data.

10. An interface for synchronous data transfer between domains clocked at different frequencies, comprising:

a first latch for receiving data from a first domain clocked at one frequency when said first latch is selected;

a second latch for receiving data from the first domain when said second latch is selected; and

a third latch for transferring data from either said first latch or said second latch to a second domain clocked at another frequency.

11. The interface of claim 10, wherein the first domain is clocked at a faster frequency than the second domain and wherein said third latch will transfer data to the second domain from said first or second latches when the second domain is clocked by a next clock pulse.

12. The interface of claim 11, wherein said third latch is alternately toggled to transfer data from said first latch or said second latch in response to a negative edge of a clock pulse clocking the second domain.

13. The interface of claim 10, wherein the first domain is clocked at a slower frequency than the second domain and wherein said third latch will transfer data to the second domain from said first or second latches is loaded when the second domain is clocked by a next clock pulse that is not a non-operate pulse.

14. The interface of claim 13, wherein said third latch is alternately toggled to transfer data from said first or said second latch in response to a negative edge of a clock pulse clocking the second domain unless the clock pulse is a non-operate clock pulse.

15. A method for synchronous data transfer between clocked domains, comprising:

loading a first master latch with data from the first domain in response to a first domain clock pulse;

transferring the data loaded in the first master latch to the second domain through a slave latch in response to a second domain clock pulse;

toggling the slave latch to switch to receive data from a second master latch in response to a negative edge of the second domain clock pulse that is not a non-operate clock pulse;

loading the second master latch with data from the first domain in response to another first domain clock pulse;

transferring the data loaded in the second master latch to the second domain through the slave latch in response to another second domain clock pulse;

toggling the slave latch to switch to receive data from the first master latch in response to the negative edge of the clock pulse of the second domain clock that is not a non-operate clock pulse;

repeating a cycle of alternately loading the first and second master latches and

transferring data to the second domain through the slave latch until a master clear signal is received by the slave and master latches; and

entering a non-operate state during each repeated cycle for at least one clock pulse of the faster domain clock, if the domains are clocked at different frequencies.

16. The method of claim 15, further comprising: generating a signal in response to loading one of the first or second master latches to cause data to be loaded alternately into the first and second master latches.

17. The method of claim 15, wherein each repeated cycle is framed by a synch pulse derived from a primary clock.

18. The method of claim 15, wherein the non-operate state is selected to minimize latency in transferring the data between the domains.

19. The method of claim 15, wherein the clock pulses of the first domain and the second domain are both derived from a primary clock and repeat in a ratioed, systematic pattern framed by a secondary synch pulse.